

## iDDS-1-SE (single output) iDDS-2-SE (dual output)



# Programmable Frequency Synthesizer

1106

### Description

The iDDS programmable frequency source comprises of three key functional areas: a 16-bit micro controller (uC) with non-volatile FLASH memory, user programmable SRAM and up to two Direct Digital Frequency Synthesisers.

The iDDS is programmed and controlled via a PC serial port. Once programmed, a power-on function is available to boot-up the iDDS without the need for user intervention or host PC connection. Visual Basic Windows operating software is provided.

The iDDS can accept up to a maximum of 48-bits of Frequency data, 12-bits of amplitude data, 14-bits of phase data and 8-bits of control data. Through a number of operating modes, the iDDS offers the user a wide variety of frequency generation options. Model iDDS-1 features a single RF output and model iDDS-2 has a dual output capability.

#### **DIRECT Mode**

The iDDS is controlled directly from the Host PC or via a boot-up routine.

The two outputs of the iDDS-2 dual version can be set independently.

Available Functions:

- Single tone (static frequency) output.
- Zero to Max Amplitude control.
- 0-360deg phase shift between outputs for the iDDS-2
- Differential frequency offset between the two outputs of the iDDS-2

Frequency tuning response is limited by the serial comms baud rate (115K) and the data resolution.

#### **CHIRP Mode**

The iDDS is programmed from the Host PC and then operated via a boot-up routine.

A chirp is generated by rapidly incrementing the frequency. The increment step value and dwell time per increment are user programmable. Available Functions:

- Frequency Chirp (or Sweep), Up or Down  
*Plus*
- Static or ramp amplitude control

The Chirp mode offers the fastest frequency sweep capability, with a minimum dwell time of 6.7nsec per frequency increment. In this mode, phase and amplitude settings remain constant across the sweep.

Once programmed, a single trigger input is all that is required to initiate a defined frequency sweep.

#### **IMAGE Mode**

The iDDS output is controlled from user programmable SRAM memory within the iDDS. This memory is programmed from the Host PC or via a custom boot-up routine. Data is stored in sets. Each set comprises of 16bit Frequency, 12bit Amplitude, Phase and Ancillary control data. When outputting, the memory is addressed in sequence. The RF signal responds to a new data set at each valid update clock input. This update clock rate is under user control.

Any frequency profile can be down loaded including uni-directional, bi-directional and random frequency patterns. The key advantage of this mode is that specific amplitude and phase values are assigned to each frequency. This permits power vs. frequency programming plus phase steering of the RF outputs (-2 only). This latter function is ideal for Beam steered AO deflectors.

This mode is very flexible and allows a high data throughput with frequency specific amplitude (and phase) control. The minimum dwell time per frequency point is less than 1usec.

Once programmed, only the trigger and clock inputs are required to control the data output.

#### **ALL SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE**

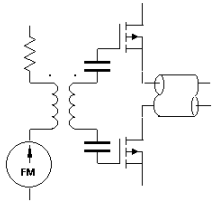
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#### **Quality Assured.**

**In-house: RF & Digital design  
Software Development  
OEM manufacture**



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**iDDS-2-SE (dual output)**



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**Specification**

Maximum Frequency Bandwidth (full range):	10 – 130 MHz	(Frequency doubled option available)
Outputs:	Model iDDS-1:	Single output, phase continuous
	Model iDDS-2:	Dual independent outputs, each phase continuous
Frequency resolution (full range):	1 Hz	
Frequency switching time (point to point) :	< 50nsec	
Frequency sweep rate (chirp mode):	7 MHz/usec, typical	
Frequency sweep rate (LUT mode):	0.5 MHz/usec, typical	
Frequency stability (internal reference clock):	+/- 50ppm	
Phase control (Dual output version):	+/- 180deg differential between outputs	
Maximum Output Power:	+3dBm typical. (2mW)	
Output power flatness:	< +/- 1dB	
Harmonics:	> 25dBc	
Power adjustment range:	10dB via pre-set potentiometer	
Amplitude modulation resolution:	12 bit (zero to potentiometer set point)	
DC Supply:	+5V @ 4A, +12V or +15V @ 200mA, -12V or -15V @ 200mA	
Comms port:	RS232 at 115Kbaud (Option: RS485) Factory set	
Memory capacity:	16K frequency data points	
Mechanical package:	Aluminium shielded case with integral fan. See diagram below	

**Auxiliary I/O features**

The iDDS also features up to 18 analog and 20 digital I/O signals offering a variety of programmable test and control options

- Three independent 12-bit DAC's,
- Fifteen 10-bit ADC inputs.
- Eight user defined I/O logic signals.
- Four logic input signals with interrupt capability.
- Five differential, opto-isolated inputs
- Three differential, opto-isolated outputs

**Options**

- F** : Frequency Doubled output
- A** : Voltage input via J6 controls the output frequency (Pseudo VCO mode)
- P** : 8bit parallel input via J4, selects 1 of 256 pre-defined output frequencies
- L** : Internal memory configured to give 64 pages of 290 frequency data points
- M** : Increased memory allowing 64K data points
- D** : Differential input logic on I/O signals

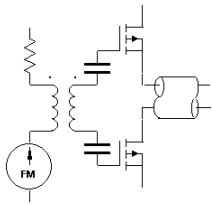
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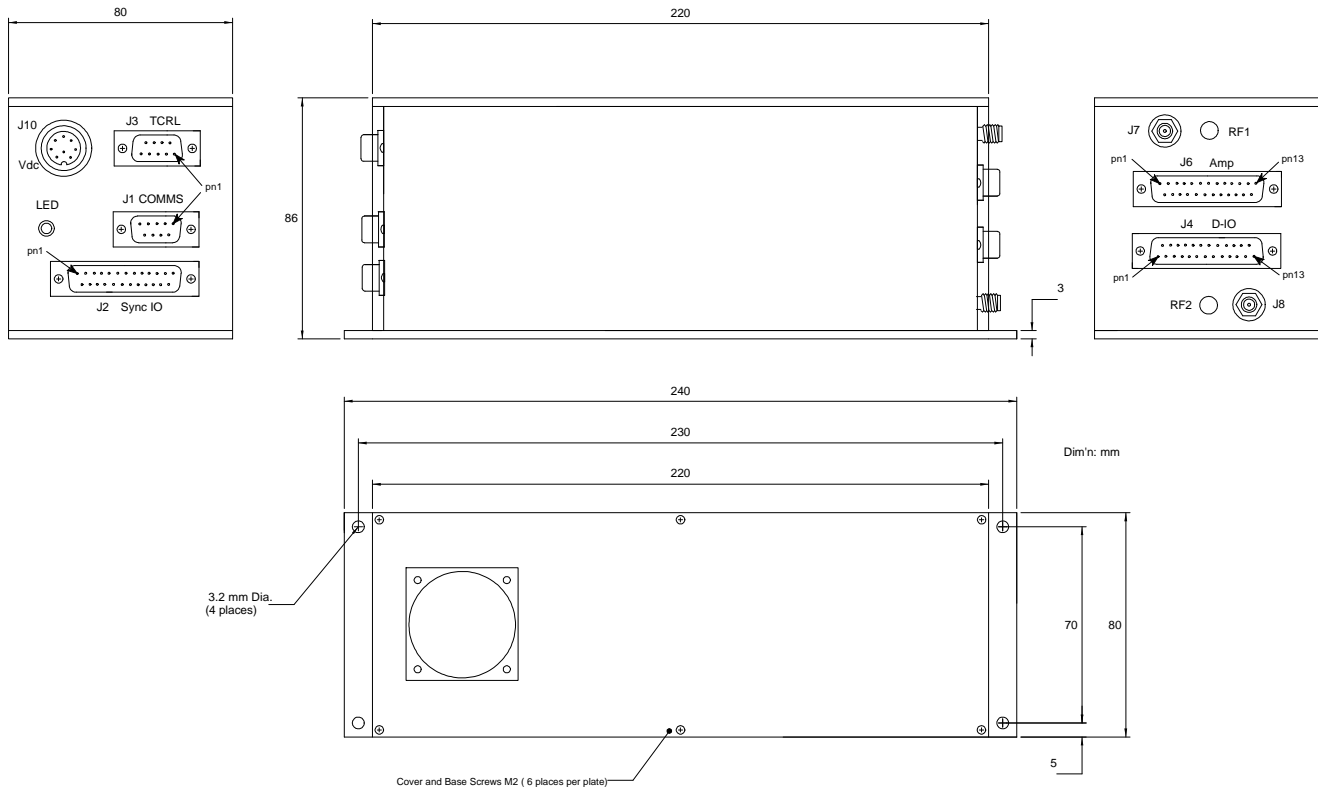
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### OUTLINE DRAWING



Dual output model iDDS-2 illustrated. The output RF2/J8 does not apply to the single output models

### Connector Summary

All 'D-type' Connectors include PI filters.

- J1:** 9-way male D-type, RS232 serial communication
- J2:** 25-way male D-type, Synchronous I/O Signals, Clock and Trigger inputs,
- J3:** 9-way female D-type, Analog I/O Signals
- J4:** 25-way female D-type, Asynchronous IO Signals
- J6:** 25-way male D-type, ADC Input Signals, opto-isolated outputs
- J7:** SMA, RF1 output
- J8:** SMA, RF2 output. Phase controlled
- J10:** 5-way Circular Panel Plug, Binder 680, DC supply input (+5Vdc/4A, +/-12Vdc/0.2A)

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